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		Application Number		10-625,065	
		Filing Date		07-22-03	
		First Named Inventor		Jong-Jan Lee	
		Group Art Unit		1763	
Examiner Name		Goudreau			
Sheet	1	of	1	Attorney Docket No.	SLA.0696

U.S. PATENT DOCUMENTS						
Examiner Initials	Cite No. ¹	U.S. Patent Document Kind Number	Code ² (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YY	Pages, Columns, Lines, Where Relevant Passages or Figures Appear

FOREIGN PATENT DOCUMENTS								
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, country where published, source.	T ²
gag		M. JURCZAK ET AL., SON (Silicon on Nothing) - A New Device Architecture for the ULSI Era, VLSI Tech. Dig., p.29, (1999).	✓
		R. KOH, Buried Layer Engineering to Reduce the Drain-Induced Barrier Lowering of Sub-0.05um SOI-MOSFET Jpn. J. Appl. Phys., Vol. 38, P. 2294 (1999)	✓
		M. JURCZAK, ET AL., Silicon-on-Nothing (SON) - an innovative Process for Advanced CMOS, IEEE Trans. El. Dev. Vol. 47, pp2179-2187 (2000).	✓
		R. CHAU ET AL., A 50nm Depleted-Substrate CMOS Transistor, IEDM, p. 621, 2001.	✓
gag		T. SATO ET AL., SON (Silicon on Nothing) MOSFET Using ESS (Empty Space in Silicon) Technique for SoC Application, IEDM, p. 809, 2001.	✓

Examiner Signature	George Goudreau	Date Considered	4-05'
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Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
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